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ABSTRACT

The performance of a Ka-Band PIN-diode switch, configured in double-ridged WR-28 waveguide and composed of up to six contiguous, self-contained modules is described. The large isolation, greater than 70 dB in the OFF state, while maintaining 1 dB minimum insertion loss in the ON state, is obtained through the application of the traveling-wave concept. The switch at present exhibits in excess of 10% bandwidth near 35 GHz in both states. Switching times of the silicon mesa diodes, measured on several completed assemblies, is 10-15 nanoseconds from OFF to ON state and less than five nanoseconds in the reverse sequence.

These results are compared with predictions based on a cascaded circuit model using measured diode, parasitic and transmission line elements. The empirical relationship of peak power and switching times in PIN-diodes are used to predict the performance of a fully developed Ka-Band PIN-diode switch.

INTRODUCTION

Amplitude and phase modulation of microwave power with semiconductor diodes has been in common practice for many years (1,2). At millimeter wavelengths, single diodes switches have been developed to deliver in excess of 100 milliwatts of modulated power with sub-nanosecond switching speed over relatively narrow passbands (3,4). The series connection of eight diodes in a fin line circuit for low power switching throughout Ka-band has recently been demonstrated with 50 dB isolation (5).

The periodically loaded waveguide has been amply treated in the literature as a structure in which traveling waves may interact discretely with electron beams (6) as well as with semiconductor diodes (7). When periodically loaded with PIN diodes, this transmission line is uniquely suited to produce arbitrarily large on-off ratio as a mm-switch with low insertion loss.

THE TRAVELING WAVE PIN-DIODE SWITCH

When a smooth waveguide is loaded along its axis with periodically spaced shunt obstacles, such as pin-diodes, the waveguide high pass characteristic becomes a bandpass filter with alternating stop and passbands as a function of obstacle spacing shown in Figure 1. Diode spacing is arranged so that the ON (low insertion loss) and OFF (high reflection loss) states of the resulting switch coincide with a passband and stopband, respectively. The double-ridged waveguide (WR-28) was chosen as a circuit that has both excellent heat transfer as well as the ability to concentrate the RF fields in the region of the switching element. The periodically-spaced diodes, placed in shunt across the narrow gap (gap height = 0.457 mm) of the central ridges may then be contained in a one-diode-per-section arrangement that permits easily controlled diode insertion and access for inspection of the assembled module as may be seen from Figure 2. Many such modules can be cascaded to provide the required isolation. An experimental hardware implementation consists of five self-contained

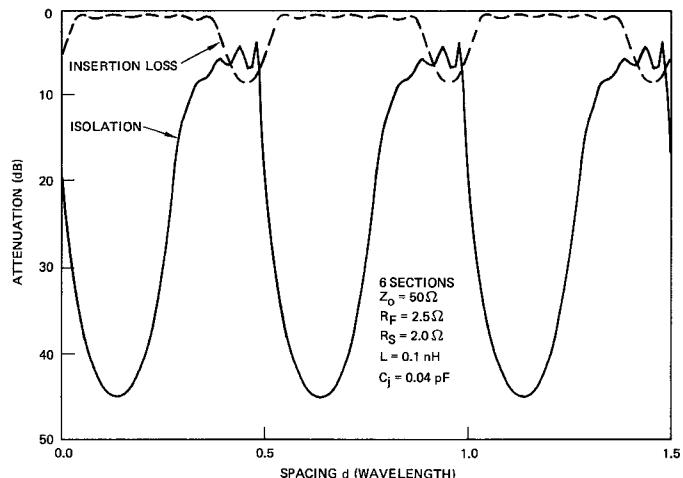


Figure 1. Pass & Stop Bands in Two States of Diode-Loaded Waveguide

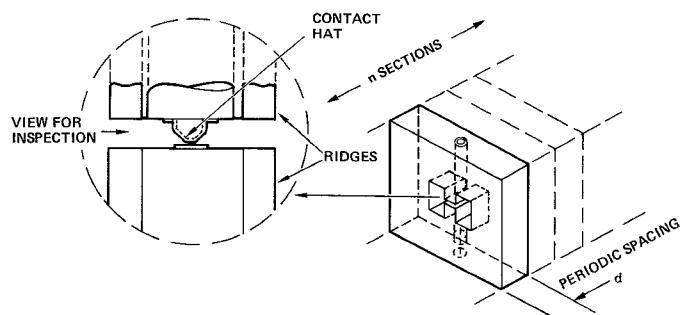


Figure 2. Cascading n Self Contained PIN Diodes

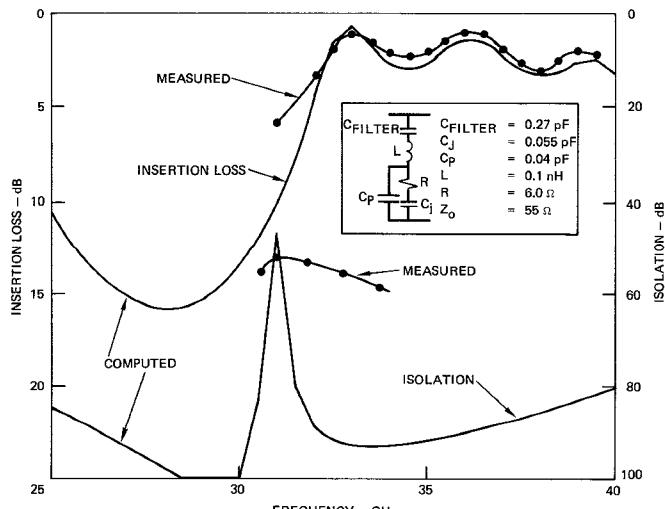


Figure 3. Small Signal Frequency Response of Six-Section Pin Diode Switch

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diode modules as well as two step-transformers. These were especially developed for the required impedance transformation between WR-28 standard and dc double-ridged waveguides.

Guidelines for this exploratory switch development were provided by a modest computer program that is based on the lumped-element circuit model for the semiconductor devices cascaded to simulate a switch containing n diode modules. With the aid of this program, the performance may be computed versus parameter variation and to explore the optimum diode-spacing for a given set of diode circuit element values. As an example, the alternating pass and stop band attenuation of a six-section assembly was shown previously in Figure 1, versus the module period d , expressed in wavelengths and for an assumed set of equivalent circuit elements and waveguide impedance. In the passband (low insertion loss) calculation, the diode is assumed in reverse bias ($V_R \approx -10$ Volts), while the stop band (isolation) results from a forward biased diode, where the waveguide is periodically shunted by the diode forward resistance ($R_S = 2\Omega$) in series with a parasitic inductance ($L = 0.1$ nH). Pass and stop bands are seen to repeat every half wavelength, a feature that permits the construction of a practical traveling wave PIN-diode switch at mm wave frequencies. Adequate spacing for the placement of bias and switching networks dictate the use of the second stop band with module period d in Figure 2 of about 0.62 guide wavelength at 35 GHz.

PIN-DIODE SWITCH PERFORMANCE - SMALL SIGNAL

The small-signal swept frequency response of an early experimental switch assembly, containing six modules is shown in Figure 3. In addition the predicted performance for the forward and reverse-biased diode states are also shown for comparison. The equivalent circuit used in this computation lists both measured diode series circuit values (L , R and C_J), as well as parasitic shunt capacitance C_p and a series tuning capacitance that is derived from the DC-bias filter. The impedance of the double-ridged waveguide, in which the diodes are imbedded is computed for a ridge gap of 0.457 mm.

The equivalent circuit parameters for the diode junction capacitance and the parasitic reactances were obtained from measurements and from forward optimization of the frequency response based on a discrete approximation to the distributed parasitic reactances associated with the cone-shaped mesa contact post, shown in Figure 4. The developmental Si PIN-diode chip on its integral circular Cu heatsink is seen in Figure 4a. An enlarged SEM micrograph (Figure 4b) shows the mesa configuration in detail. Finally, the assembled diode section as seen looking into the ridged guide gap is shown in Figure 4c. The contact hat (an approximation to a

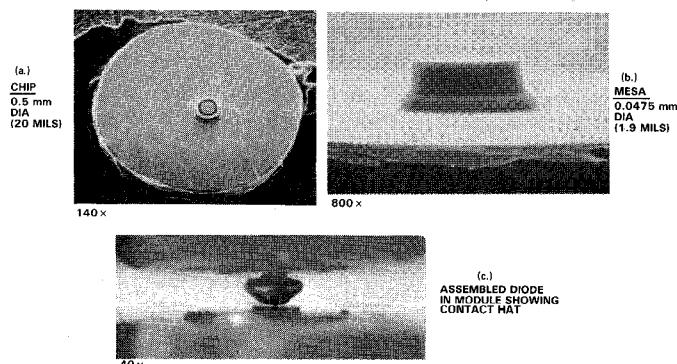


Figure 4. Detailed Views of Developmental PIN Diode Chip, Mesa and Assembly in Ridged Gap

45 degree half angle cone) is of bellows construction, designed to prevent excessive applied force to the mesa and yields near minimum parasitic reactance that is mandatory for low insertion loss and large relative bandwidth.

The close agreement in insertion loss between the measured and predicted frequency responses is evidence of a realistic assessment of the diode equivalent circuit. However, the measured isolation is substantially lower than the computed response. While not shown beyond 34 GHz, isolation at higher frequencies is in excess of 60 dB, the highest measurable attenuation value in our test station. The large discrepancy results quite possibly from inaccurate modeling of the double-ridged waveguide, in which evanescent higher order modes are excited. These are not accounted for in the present transmission line formulation. Thus, the computed isolation may be considered as an upper limit.

Further exploratory development produced a number of five-module PIN-diode switches that were assembled under relatively controlled conditions. The small-signal swept frequency response of one of these is shown in Figure 5. These switches showed much

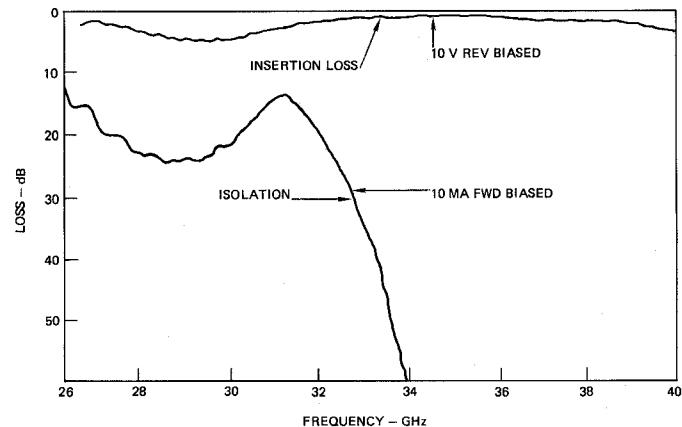


Figure 5. Isolation and Insertion Loss versus Frequency - 5-Section Pin Diode Switch No. 2

improved and reproducible performance as can be seen from Table I that lists the performance of four switches. The minimum terminal insertion loss (at f_{min}) is less than 1 dB for all assemblies with ample bandwidth for most systems requirements. The

TABLE I. PERFORMANCE SUMMARY

1	2	3	4	5	6
Switch No.	f_{min} (GHz)	I.L. (dB)	$\Delta f(1)$ (GHz)	ISO.(3) (dB)	$f_{min}(2)$ (GHz)
1	34.5	0.9	3.2	60	33.7
2	34.5	0.8	5.7	60	34.0
3	33.4	0.95	4.5	60	33.4
4	33.2	0.85	3.6	60	33.8

NOTES:

- 1) 1 dB bandwidth
- 2) Frequency of minimum isolation
- 3) Isolation is in excess of 70 dB from 34-38 GHz in switch No. 4, by point-to-point measurement

frequency for onset of greater than 60 dB isolation is surprisingly uniform near 33.7 GHz. The higher than 60 dB isolation was obtained by series resonance of the mesa contact inductance and the capacitance

associated with the DC-bias network. The contribution of the switch assemblies, after subtraction of the two step transformer losses ranges from 0.6 - 0.8 dB.

PIN-DIODE SWITCH PERFORMANCE - LARGE SIGNAL

Performance under elevated peak and average power conditions was explored to obtain preliminary data on limiting factors. All tests were of the "cold switching" variety, so that RF power was removed from the switch input prior to switching between ON and OFF states. Pulse repetition and switching frequencies were in the 1 MHz range. The RF duty cycle was varied from less than 5 to 50 percent depending on the purpose of the particular test to assess peak or average power limitations. Power levels up to 100 watts at 35 GHz were available through the use of a high power traveling wave amplifier in our test station. All tests were intentionally carried to failure in these early developmental devices. Table II lists the terminal stress conditions for each of these test sequences in which at least one of the diodes failed catastrophically, usually as a short circuited mesa. Sequences 1 - 3 may be

TABLE II. POWER TEST RESULTS

Test Sequence	Peak Power Watts	Duty Cycle %	Pulse Duration μ sec
1	25	30	0.375
2	30	50	0.375
3	40	30	0.375
4	100	5	0.062

considered average power failures, as estimated from mesa temperatures that reached nearly 2000°C. Test sequence 4 was terminated by what is considered a peak power failure at 115 watts, based on a) the estimated instantaneous peak inverse voltage across the PIN region to produce a failure mode (see later), b) the short pulse duration compared to the computed thermal time constant of the mesa ($\approx 1 \mu$ sec), c) the fact that the estimated mesa temperature near 1000°C was not exceeded, and d) onset of power saturation, evidenced by increased insertion loss that was observed at the highest operational peak power of 85 watts in this sequence (not shown).

PEAK POWER AND SWITCHING TIME LIMITATIONS

The interdependence of peak RF power P_p , reverse breakdown voltage V_{BD} , and switching time τ_s (rise or fall time τ_s between ON and OFF states) for Si PIN-diodes was developed in unpublished work on a strictly empirical basis. Reported experimental results⁽²⁾ suggest a relationship between these parameters, given by

$$\tau_s \approx 1.25 \times 10^{-2} (12W)^{3/2} \text{ (nanoseconds)} \quad (1)$$

where $W = V_{BD}/12$ is the intrinsic region width in μ m. (1) assumes that a) V_{BD} for epitaxially grown intrinsic (I) regions is 12 volts per μ m of I-region width and b) the rise or fall time is $0.1 \tau_L$, where τ_L is the minority carrier life time of the particular PIN-diode used in the development. Reasonable assumptions regarding reverse bias voltage V_{BIAS} ($\approx 0.13 V_{BD}$) and peak inverse voltage V_{PI} ($\approx 0.75 V_{BD}$) lead to a relationship with the peak RF power through $V_{RF} = (2 P_p Z_0)^{1/2}$. Together with (1), the relationship is given by

$$\tau_s \approx 2.55 \times 10^{-2} (2 P_p Z_0)^{3/4} \text{ nanoseconds.} \quad (2)$$

where P_p is the peak RF power in watts and Z_0 is the characteristic impedance of the ridged waveguide. The developmental PIN-diode chips, with $W = 8 \mu$ m exhibited approximately 10 nsec switching time, in keeping with (1) above. They were expected to, and did fail due to excessive V_{PI} according to the previous discussion, when exposed to peak power levels near 100 watts.

Reliable accommodations of 100 watt peak power in a modular PIN-diode switch can be estimated from (1) and (2) above to require an intrinsic region width $W \approx 16 \mu$ m and to exhibit ON/OFF transition times near 30 nsec. Thermal analysis, beyond the scope of this paper, of a fully developed PIN-diode switch, suggests that this power level may be accommodated by these PIN-diodes in the double-ridge waveguide circuit with a duty cycle approaching 50 percent and at pulse repetition frequencies in the 1 MHz range.

SUMMARY AND CONCLUSIONS

A 35-GHz multi-section PIN-diode switch, configured in cascaded modules, each containing one silicon PIN-diode chip was developed and briefly described in this paper. The work was guided by a modest, yet versatile computer program that simulates quite closely the n-cascaded double-ridged waveguide modules and the PIN-diode equivalent circuit. It was possible to optimize both insertion loss and isolation simultaneously over a greater than 10 percent frequency band by minimizing the parasitic reactances associated with diode chip and mesa contact lead. This condition was clearly predicted by the computer optimization procedure.

Further, an empirical interdependence between peak power and switching time was developed that limits high power mm-wave switch performance. From this design relationship and thermal modeling it was possible to project the high power performance of a fully developed 35 GHz PIN-diode switch component.

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